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Substitute for form 1449B/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

Date Submitted: December 16, 2003

(use as many sheets as necessary)

Sheet

1

of

2

Complete if Known

Application Number	09/722,474
Filing Date	12/28/2000
First Named Inventor	Tomoharu TANAKA
Group Art Unit	2824
Examiner Name	V. Le
Attorney Docket Number	016887-1026

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
Ju	A1	4,794,564		WATANABE	12-27-1988	
	A2	5,297,096		TERADA ET AL.	03-22-1994	
	A3	5,357,462		TANAKA ET AL.	10-18-1994	
	A4	5,379,256		TANAKA ET AL.	01-03-1995	
	A5	5,544,117		NAKAYAMA ET AL.	08-06-1996	
	A6	3,917,933		SCHEUNEMAN ET AL.	11-04-1975	
	A7	4,456,995		RYAN	06-26-1984	
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	A13	5,436,913		YAMAMURA ET AL.	07-25-1995	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
Ju	A14	JP	59-110096	A	MITSUBISHI ELECTRIC CORP.	06-25-1984		Transl.
Ju	A15	JP	2-142000	A	HITACHI CORP. ET AL.	05-31-1990		Transl.

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
Ju	A16	K. Arimoto et al., "A Speed-Enhanced DRAM Array Architecture with Embedded ECC", IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, Feb. 1990, pages 11-17..	
Ju	A17	K. Kobayashi et al., "A High-Speed Parallel Sensing Architecture for Multi-Megabit Flash E ² PROM's", IEEE Journal of solid-State Circuits, Vol. 25, No. 1, Feb. 1990, pages 79-83.	
Ju	A18	M. Momodomi et al., "An Experimental 4-Mbit CMOS EEPROM with a NAND-Structured Cell", IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, Oct. 1989, pages 1238-1243.	

Examiner Signature

Vu le

Date Considered

02/19/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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		Attorney Docket Number	016887-1026

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ge	A19	M. Momodomi et al., "A High Density NAND EEPROM with Block-Page Programming for Microcomputer Applications", Proceedings of the IEEE 1989 Custom Integrated Circuits Conference, May 15-18, 1989, pages 10.1.1-10.1.4.	
ge	A20	T. Tanaka, et al., "A Quick Intelligent Program Architecture for 3V-only NAND-EEPROMs", 1992 Symposium on VLSI Circuits, Digest of Technical Papers, pages 20-21.	
ge	A21	M. Asakura et al., "An Experimental 1-Mbit Cache DRAM with ECC", IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, Feb. 1990, pages 5-10.	
ge	A22	R. Vancu et al., "Section 4: Nonvolatile and Fast Static Memories: A 35 ns 256k CMOS EEPROM with Error Correcting Circuitry", 1990 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, Feb. 1990, pages 64-65	
ge	A23	Lexar Media, Inc.'s Corrected Answer to Toshiba corporation's Amended Complaint for Patent Infringement, Case No. C03-00167 CRB, March 5, 2003, pages 1-13.	
ge	A24	Lexar Media's Amended Patent Local Rules 3-3 and 3-4 Disclosures, Case No. C03-00167, October 16, 2003, pages 1-33 with Exhibits A-I.	
ge	A25	C.L. Chen et al., "Error-Correcting Codes for Semiconductor memory Applications: A State-of-the-Art Review", IBM J. Res. Develop., Vol. 28, No. 2, March 1984, pages 124-134.	

Examiner Signature	V. Le	Date Considered	02/19/04
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